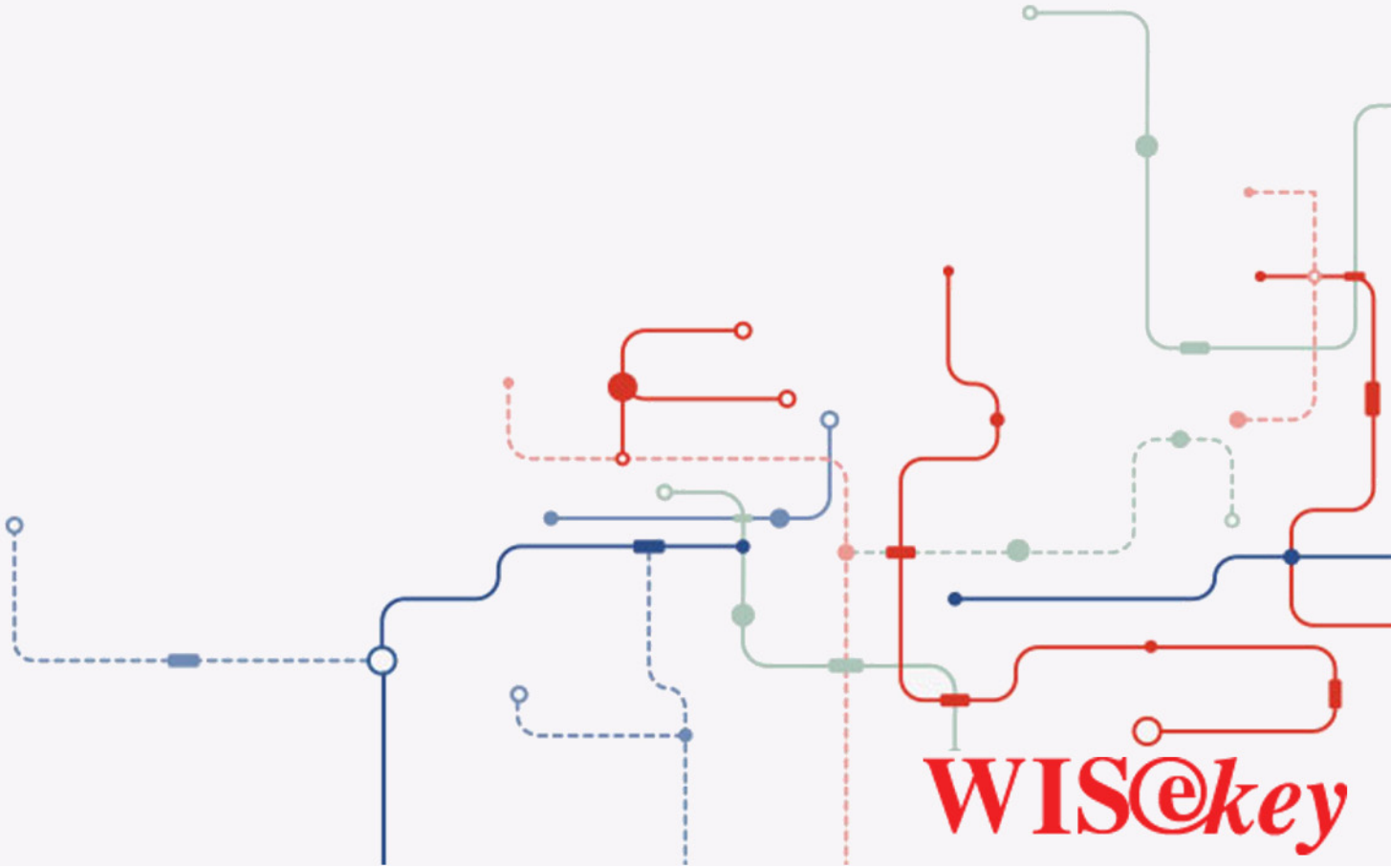
AT90SC104104CV

Summary Datasheet



Features

General

- High-performance, Low-power 8-/16-bit Enhanced RISC Architecture Microcontroller
  - 135 Powerful Instructions (Most Executed in a Single Clock Cycle)
- Low Power Idle and Power-Down Modes (GSM Compliant, <100µA in Power Down Mode)
- Bond Pad Locations Conforming to ISO 7816-2
- ESD Protection to ± 4000V
- Operating Ranges: 1.62 to 5.50V (Class A,B & C)
- Compliant with EMV 4.2 Specifications, CQM, GSM, 3GPP and PC Industry Compatible
- Available in Wafers, Modules, and Industry-standard Packages

Memory

- 104K Bytes of FLASH Program Memory
- 104K Bytes of EEPROM, Including 128 Bytes of OTP and 384 Bytes of Bit-addressable
  - 1 to 128-byte Program / Erase
  - 1.25 ms Program / 1.25 ms Erase
  - Typically 500,000 Write/Erase Cycles at a Temperature of 25°C
  - 10 Years Data Retention
  - EEPROM Erase Only Mode
  - Write EEPROM with or without AutoErase
- 8K bytes RAM Memory (6K bytes of RISC CPU Core RAM, 2K bytes of Ad-X™2 RAM, shared with the RISC CPU Core)

Peripherals

- Two I/O Ports
- Three GPIOs (shared with NFCIC Controller or HSSPI)
- One ISO 7816 Controller
  - Up to 625 Kbps at 5MHz
  - Compliant with T=0 and T=1 Protocols
- One NFCIC Controller
  - ISO 14443 Type A & B, ISO 18092, ISO 15693
  - External 13.56MHz
- Single Wire Protocol (ETSI TS 102 613 V9.20)
- High Speed SPI Interface up to 20Mbits/s (3 Pins shared with NFCIC Controller)
- Programmable Internal Oscillator (Up to 36 MHz for Ad-X2 & internal CPU Clock)
- Three 16-bit Timers
- Random Number Generator (RNG)
- 2-level Interrupt Controller
- Hardware DES and Triple DES DPA /DEMA Resistant (4 keys)
- Hardware AES
- Code Signature Module
- Checksum Accelerator
- CRC 16 & 32 Engine (Compliant with ISO/IEC 3309)
- 32-bit Cryptographic Accelerator (Ad-X2 for Public Key Operations)
  - RSA, ECDSA, ECC

Security

- Dedicated Hardware for Protection Against SPA/DPA/SEMA/DEMA Attacks
- Advanced Protection Against Physical Attack, Including Active Shield, Enhanced Protection Object, CStack Checker, Slope Detector, Parity Errors
- Environmental Protection Systems
- Voltage Monitor
- Frequency Monitor
- Temperature Monitor
- Light Protection
- Secure Memory Management / Access Protection (Supervisor Mode)

Development Tools

- Voyager Emulation Platform (ATV4+) to Support Software Development
- IAR Embedded Workbench® V5.40 Debugger or Above
- Software Libraries and Application Notes

Certification Targeted

- CC EAL5+ (PPSSVG - BSI 0002)

EMVCo

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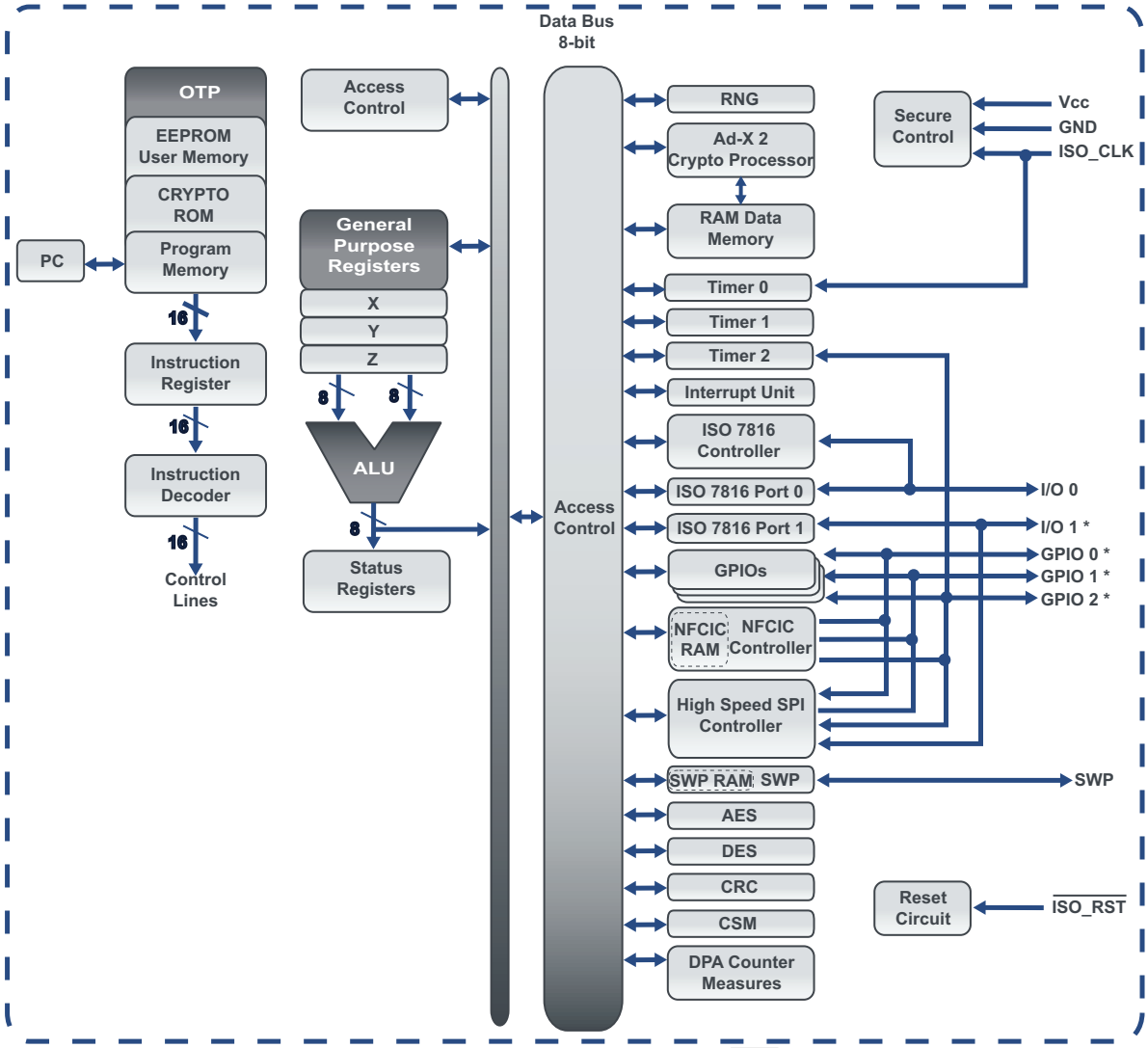
Description

The AT90SC104104CV is a low-power, high-performance, 8-/16-bit microcontroller with FLASH program memory, EEPROM memory, based on RISC architecture microcontroller.

By executing powerful instructions in a single clock cycle, the AT90SC104104CV achieves throughputs close to 1 MIPS per MHz. Its Harvard architecture includes 32 general-purpose working registers directly connected to the ALU, allowing two independent registers to be accessed in one single instruction executed in one clock cycle.

In addition to the 104K bytes of FLASH, the AT90SC104104CV includes 104K bytes of high density EEPROM. The ability to map the EEPROM in the code space allows parts of the program memory to be reprogrammed in-system. This technology combined with the versatile 8/16-bit CPU on a monolithic chip provides a highly flexible and cost-effective solution to many smart card applications.

Figure 1 AT90SC104104CV RISC CPU Core Architecture



* I/O 1 also used as $\overline{HSSS}$ for HSSPI
GPIO 0 also used as HSMOSI for HSSPI and as DIN for NFCIC
GPIO 1 also used as HSMISO for HSSPI and as DOUT for NFCIC
GPIO 2 also used as HSSPICK for HSSPI and as 13.56MHz for NFCIC

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