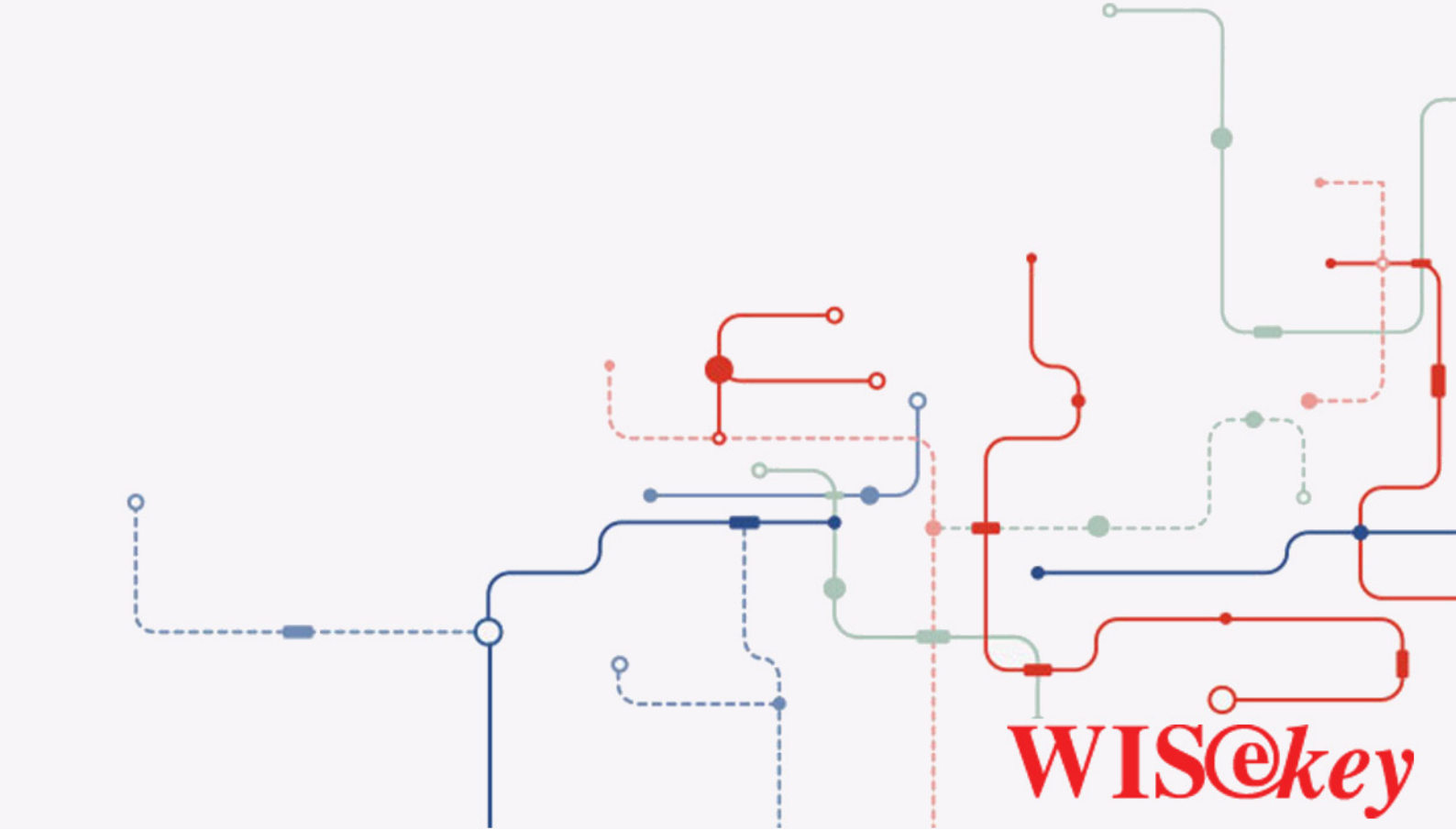
AT90SC9604RV

Summary Datasheet



Features

General

- High-performance, Low-power 8/16-Bit RISC Architecture
  - 135 Powerful Instructions (Most Executed in a Single Clock Cycle)
- Low Power Idle and Power-down Modes
- Bond Pad Locations Conforming to ISO 7816-2
- ESD Protection to ± 6000V
- Operating Ranges: 2.7 to 5.5V
- Compliant with EMV 2000 Specifications, QCM , PC Industry Compatible
- Available in Wafers, Modules, and Industry-standard Packages

Memory

- 96K Bytes of ROM Program Memory
- 4K Bytes of EEPROM, Including 64 OTP Bytes and 192 Bit-addressable Bytes
  - 1 to 64-byte Program / Erase
  - 1ms Program / 1ms Erase
  - Typically 500,000 Write/Erase Cycles at a Temperature of 25°C
  - 10 Years Data Retention
  - EEPROM Erase only mode
  - Write EEPROM with or without autoerase
- 2K bytes RAM Memory

Peripherals

- One I/O Port
- One ISO 7816 Controller
  - Up to 625 Kbps at 5 MHz
  - Compliant with T=0 and T=1 Protocols
- Programmable Internal Oscillator (Up to 30 MHz for internal CPU Clock)
- Two 16-bit Timers
- Random Number Generator (RNG)
- 2-level Interrupt Controller
- Hardware DES and Triple DES DPA/DEMA Resistant
- Checksum Accelerator
- CRC16 & 32 Engine (Compliant with ISO/IEC 3309)

Security

- Dedicated Hardware for Protection Against SPA/DPA/SEMA/DEMA Attacks
- Advanced Protection Against Physical Attack, Including Active Shield, EPO, Slope Detector, Parity Errors
- Environmental Protection Systems
- Voltage Monitor
- Temperature Monitor
- Light Protection

Certification targeted

- EMVCo

Development Tools

- Voyager Emulation Platform (ATV4) to Support Software Development
- IAR Embedded Workbench® V5.40 Debugger or Atmel's AVR Studio® Version 4.07 or Above
- Software Libraries and Application Notes

6591CS – 26Sep16

Description

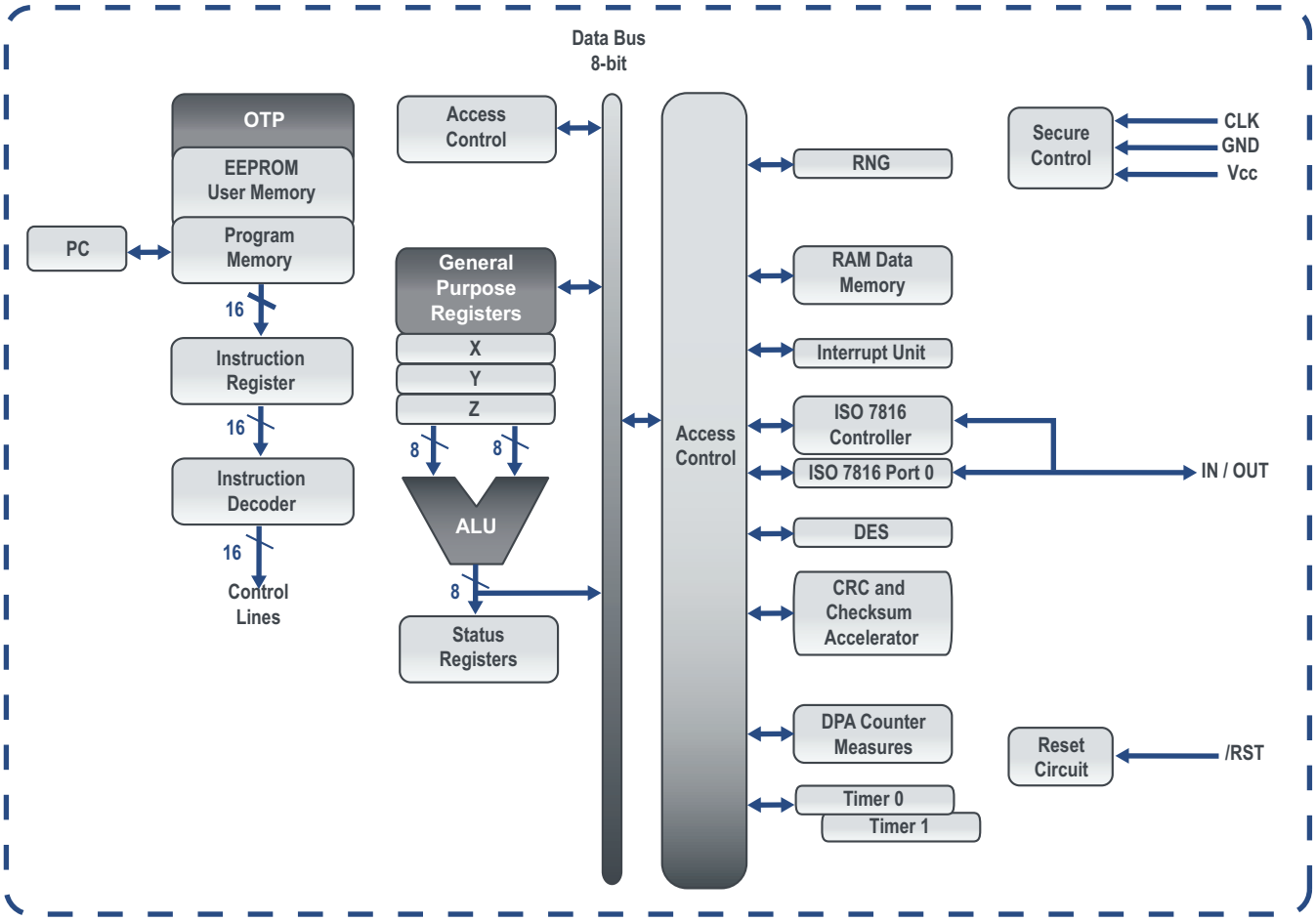
The AT90SC9604RV is a low-power, high-performance, 8/16-bit microcontroller with ROM program memory, EEPROM memory, based on the enhanced RISC architecture.

By executing powerful instructions in a single clock cycle, the AT90SC9604RV achieves throughputs close to 1 MIPS per MHz. Its Harvard architecture includes 32 general-purpose working registers directly connected to the ALU, allowing two independent registers to be accessed in one single instruction executed in one clock cycle.

In addition to the 96K bytes of embedded ROM, the AT90SC9604RV includes 4K of high density EEPROM. The ability to map the EEPROM in the code space allows parts of the program memory to be reprogrammed in-system. This technology combined with the versitile 8/16-bit CPU on a monolithic chip provides a highly flexible and cost-effective solution to many smart card applications.

As this device is based on the enhanced family, this device is compliant with EAL5+ certification.

Figure 1 Shows a block diagram of the AT90SC9604RV



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