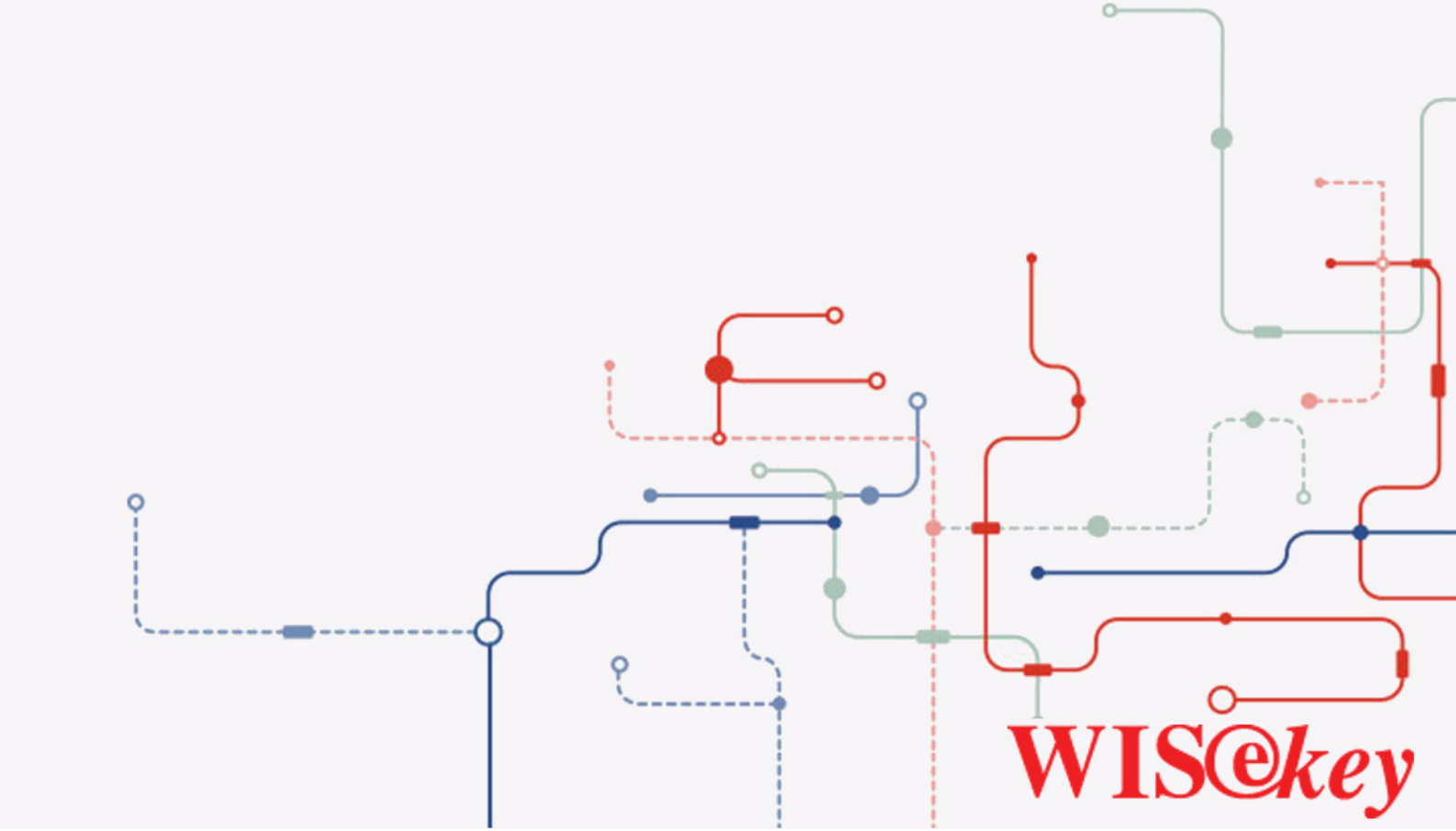
# AT90SO72

## Summary Datasheet



# Features

## General

- High-performance, Low-power 8-/16-bit Enhanced RISC Architecture Microcontroller
  - 135 Powerful Instructions (Most Executed in a Single Clock Cycle)
- Low Power Idle and Power-Down Modes
- Internal Variable Frequency Oscillator up to 36 Mhz
- Bond Pad Locations Conforming to ISO 7816-2
- ESD Protection up to ± 4000V
- Operating Range: 2.7V to 5.5V
- Operating Temperature: -40°C to +105°C
- Available in Wafers, Modules and standard ROHS packages:
  - 20-QFN (RoHS compliant) 4mm x 4mm
  - 8-SOIC (RoHS compliant) 5mm x 5mm

## Memory

- 288K Bytes of ROM Program Memory including 32K Bytes of Crypto ROM
- 72K Bytes of EEPROM, including 128 OTP Bytes and 384 Bit-addressable Bytes
  - 1 to 128-byte Program / Erase
  - 2 ms Program / 2 ms Erase
  - Typically 500,000 Write / Erase Cycles at a Temperature of 25°C
  - Typically 200,000 Write / Erase Cycles at a Temperature of 105°C
  - 10 Years Data Retention
- 8K Bytes of RAM Memory (6K Bytes of RISC CPU RAM, 2K Bytes of Cryptographic Accelerator RAM, shared with the RISC CPU core)

## Communication

- USB 2.0 Full Speed Interface
  - 6 Programmable Endpoints with IN or OUT Directions for Bulk, Interrupt or Isochronous Transfers (2 end-points with double buffering of 64x2 bytes)
  - DMA Controller for fast transfers between internal DPRAM to RAM
  - 48 MHz clock for Full-speed Bus Operation
- USB 2.0 Low Speed Interface
  - No external resonator required
- Master / Slave SPI Serial Controller
- I²C (Two Wire Interface) up to 400 Kbits/s
  - Multiple Masters supported

## Other Peripherals

- Hardware Communication Interface Detection
- Up to 7 General Purpose I/Os multiplexed with SPI and I²C interfaces
- Programmable Internal Oscillator (Up to 36 MHz for CPU and Crypto Accelerator)
- Two 16-bit Timers
- Random Number Generator (RNG)
- 2-level Interrupt Controller
- Hardware DES/TDES Engine DPA/DEMA Resistant
- Hardware AES 128/192/256 Engine DPA/DEMA Resistant
- Checksum Accelerator
- CRC 16 & 32 Engine (Compliant with ISO / IEC 3309)
- 32-bit Cryptographic Accelerator (Ad-X™2 for Public Key Operations)
  - RSA, DSA, ECC, Diffie-Hellman, Key Generation (thanks to Crypto Toolbox Library)

6597DS – 08Feb19

## Security

- Dedicated Hardware for Protection Against SPA/DPA/SEMA/DEMA Attacks
- Advanced Protection Against Physical Attack, including Active Shield, Enhanced Protection Object, CStack Checker, Slope Detector, Parity Errors
- Environmental Protection Systems
- Voltage Monitor
- Frequency Monitor
- Temperature Monitor
- Light Protection
- Secure Memory Management/Access Protection (Supervisor Mode)

## Development Tools

- Voyager Emulation Platform (ATV4+) to Support Software Development
- IAR Embedded Workbench® V5.40 Debugger or Above
- Software Libraries and Application Notes

## Certifications / Standards

- CC EAL5+
- USB 2.0

# Description

The AT90SO72 is a low-power, high-performance, 8-/16-bit microcontroller with ROM program memory, EEPROM memory, based on RISC architecture microcontroller.

By executing powerful instructions in a single clock cycle, the AT90SO72 achieves throughputs close to 1 MIPS per MHz. Its Harvard architecture includes 32 general-purpose working registers directly connected to the ALU, allowing two independent registers to be accessed in one single instruction executed in one clock cycle.

In addition to the 288K Bytes of embedded ROM, the AT90SO72 includes 72K Bytes of high density EEPROM.

The ability to map the EEPROM in the code space allows parts of the program memory to be reprogrammed in-system. This technology combined with the versatile 8/16-bit CPU on a monolithic chip provides a highly flexible and cost-effective solution to many applications.

The USB V2.0 Full Speed controller provides a dynamic pull-up attachment and detachment and a host detection mechanism.

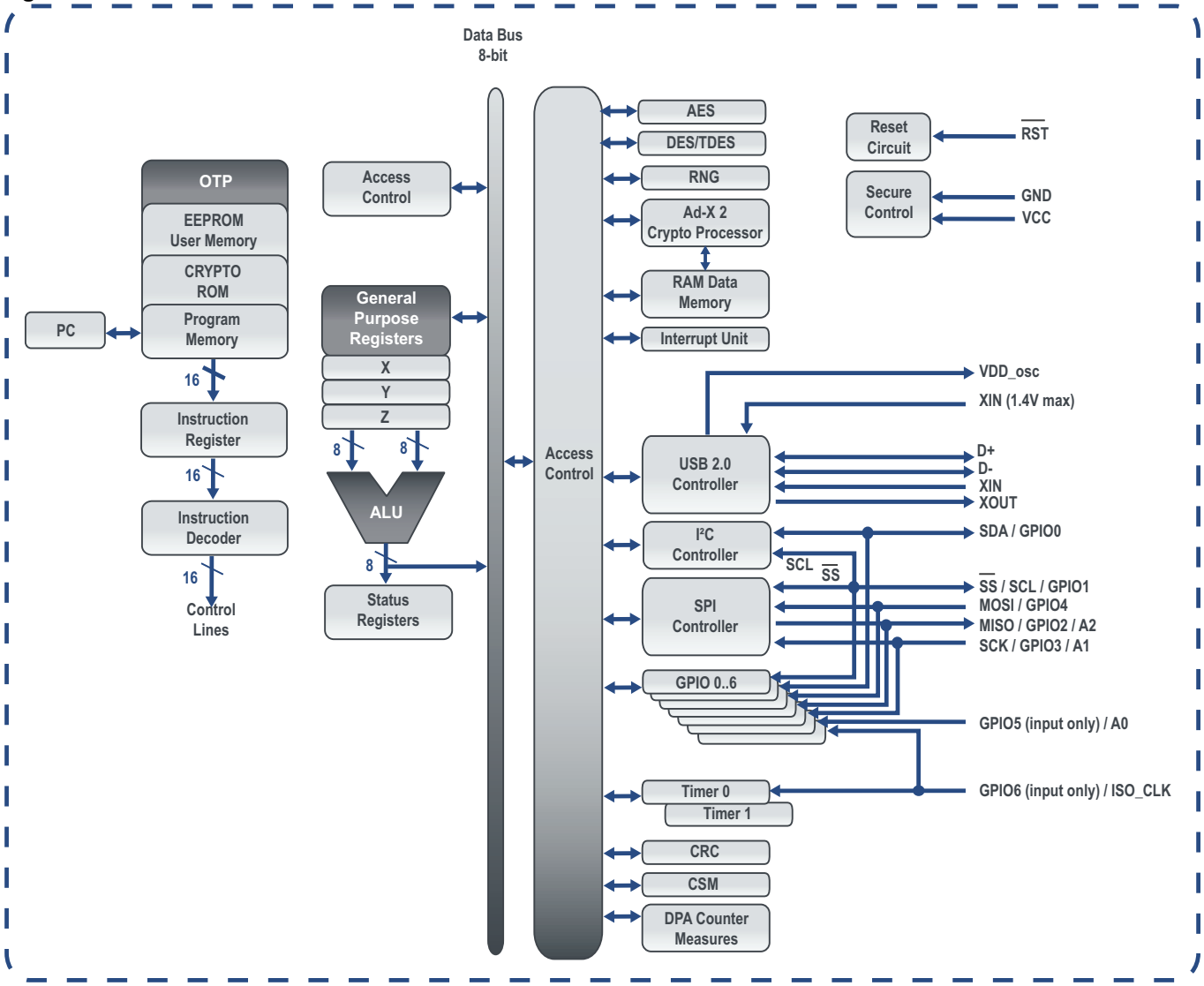
The AT90SO72 features also a USB 2.0 Low Speed interface which does not require an external resonator.

The USB interface provides six configurable data transfer endpoints, each with its own DPRAM in the memory area. The data transfer type for each endpoint is configured by software. A DMA controller allows a fast communication rate between the RAM of the CPU and the DPRAM.

The SPI interface, when configured as a master, provides a clock up to 10MHz thanks to the dedicated internal VFO clock system. The SPI controller features three sources of interrupt (Byte Transmitted, Time-out and Reception Overflow) and a programmable clock and inter-bytes (guardtime) delays.

The I²C interface interconnects components on a unique two-wire bus, made up of one clock line and one data line with speeds of up to 400 Kbits per second, based on a byte-oriented transfer format. It is programmable as a master or a slave with sequential or single-byte access. Multiple master capability is supported. Arbitration of the bus is performed internally and puts the I²C in slave mode automatically if the bus arbitration is lost. A configurable baud rate generator permits the output data rate to be adapted to a wide range of core clock frequencies.

**Figure 1** AT90SO72 RISC RISC CPU Core Architecture




**List of pins**

| | | | |
|---|---|---|---|
| A0, A1, A2 | I²C address bits (A0 as input only) | SS | SPI Slave Select |
| GND | Ground (reference voltage) | SCK | Clock signal for the SPI |
| GPIOx | General Purpose Input or Output | D+ | USB D+ differential data |
| ISO_CLK | Clock signal input to internal clock operating circuit | D- | USB D- differential data |
| MISO | SPI Master Input / Slave Ouput | VCC | Power supply input |
| MOSI | SPI Master Output / Slave Input | VDD_osc | Power supply input for Internal Oscillator |
| RST | Reset pin | XIN (1.4V max) | Oscillator signal input to generate internal clock operating circuit (1.4V max) |
| SCL | Clock Signal for Serial (I²C) | XIN | Resonator signal input to generate internal clock operating circuit |
| SDA | Input or Output for serial data (I²C) | XOUT | Resonator signal output to generate internal clock operating circuit |

# Ordering information

| Reference | Description |
|---|---|
| **AT90SO72-xxx-P** | **xxx** : Chip Personalization Number*<br>**P** = Z : QFN20 Package<br>R : SOIC8 Package |

* For more details about the Chip Personalization Number, please contact your local INSIDE Secure sales office.

# Pinouts & Packages

## Pinouts Information

| Configuration | Interfaces available (multiplexed) | Package |
|---|---|---|
| **1** | - USB Full Speed (External Resonator required)<br>- USB Low Speed<br>- I²C<br>- GPIOs | SOIC8 |
| **2** | - USB Low Speed<br>- USB Full Speed (External Oscillator required)<br>- I²C<br>- GPIOs | SOIC8 |
| **3** | - USB Low Speed<br>- USB Full Speed (External Resonator required)<br>- SPI<br>- I²C<br>- GPIOs | QFN20 |
| **4** | - USB Full Speed<br>- GPIOs | SOIC8 |
| **5** | - SPI<br>- I²C<br>- GPIOs | SOIC8 |
| **6** | - SPI<br>- I²C<br>- ISO7816<br>- GPIOs | QFN20 |

**Figure 1** AT90SO72 pinout configuration 1

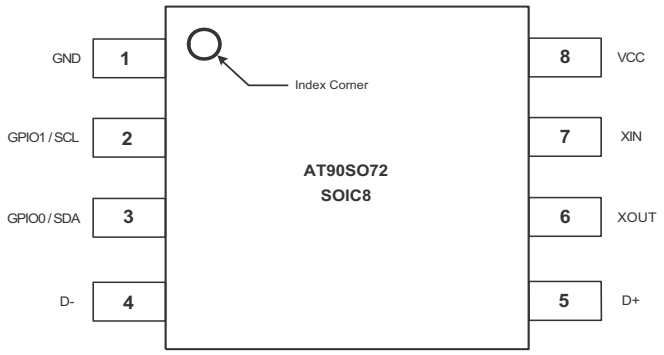



**Figure 2** AT90SO72 pinout configuration 2

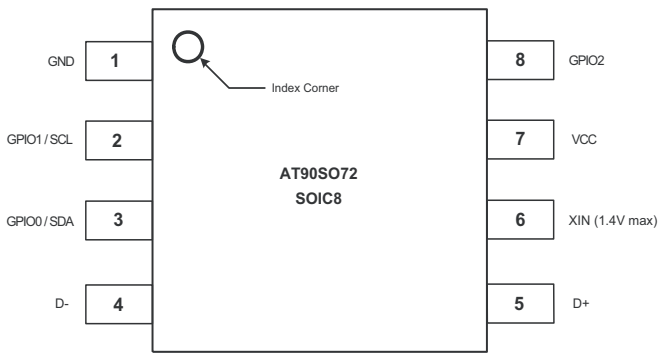


**Figure 2** AT90SO72 pinout configuration 3

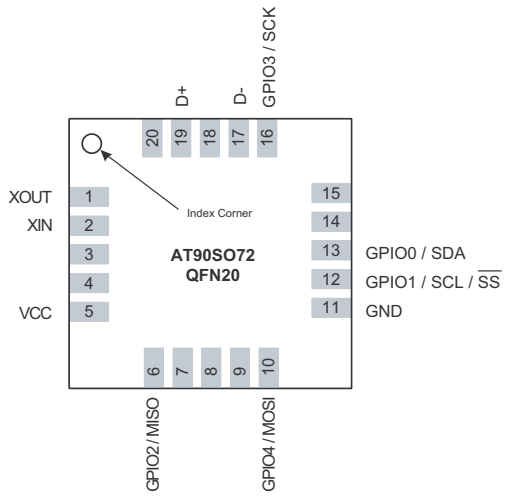



**Figure 3** AT90SO72 pinout configuration 4

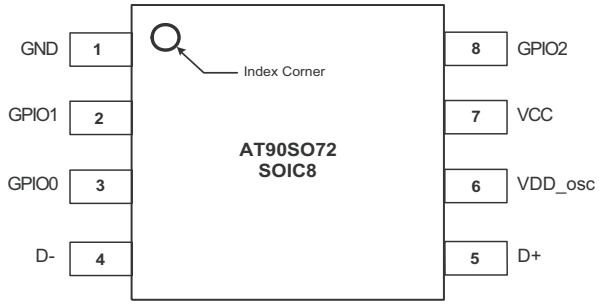



**Figure 4** AT90SO72 pinout configuration 5

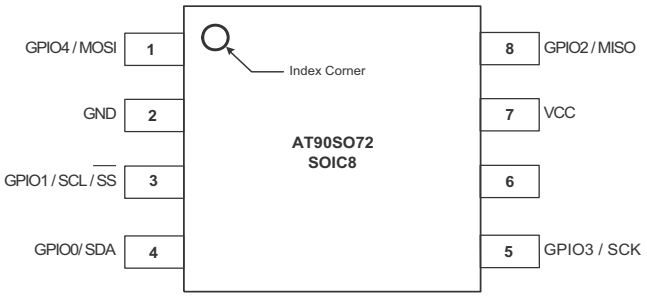
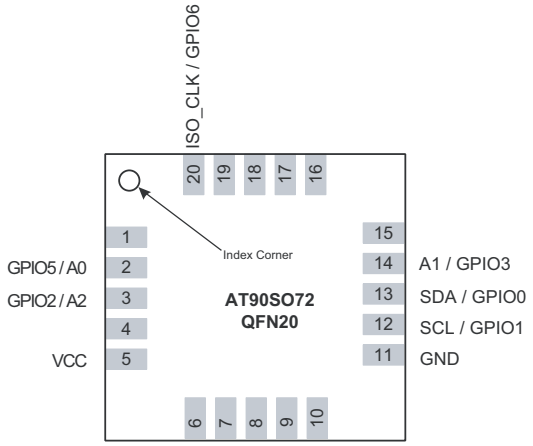



**Figure 5** AT90SO72 pinout configuration 6



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