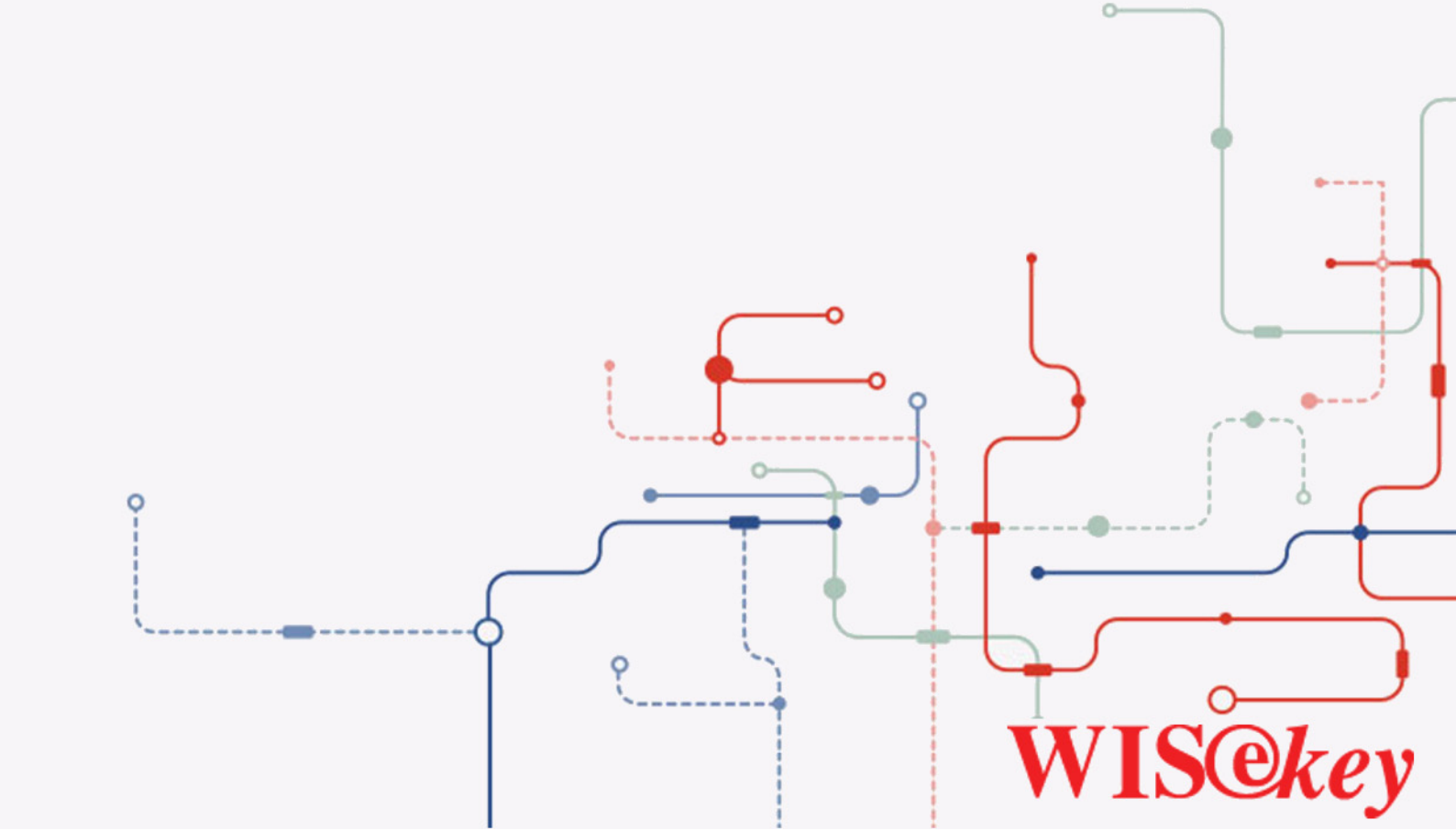
AT90SO128

Summary Datasheet



Features

General

- High-performance, Low-power 8-/16-bit Enhanced RISC Architecture Microcontroller
  - 135 Powerful Instructions (Most Executed in a Single Clock Cycle)
- Low Power Idle and Power-Down Modes
- Internal Variable Frequency Oscillator up to 35 Mhz
- Bond Pad Locations Conforming to ISO 7816-2
- ESD Protection up to ± 4000V
- Operating Range: 2.7V to 5.5V
- Operating Temperature: -25°C to +85°C
- Available in Wafers, Modules and standard ROHS packages:
  - 44-QFN (RoHS compliant) 7mm x 7mm
  - 8-SOIC (RoHS compliant) 5mm x 5mm

Memory

- 288K Bytes of ROM Program Memory including 32K Bytes of Crypto ROM
- 128K Bytes of EEPROM, including 128 OTP Bytes and 384 Bit-addressable Bytes
  - 1 to 128-byte Program / Erase
  - 2 ms Program / 2 ms Erase
  - Typically 500,000 Write / Erase Cycles at a Temperature of 25°C
  - 10 Years Data Retention
- 12K Bytes of RAM Memory (10K Bytes of RISC CPU RAM, 2K Bytes of Cryptographic Accelerator RAM, shared with the RISC CPU core)

Communication

- One ISO 7816 Controller
  - Up to 625 kbps at 5 MHz
  - Compliant with T = 0 and T = 1 Protocols
- High Speed Master / Slave SPI Serial Interface up to 20 Mbits/s
- I²C (Two Wire Interface) up to 400 Kbits/s
  - Multiple Masters supported
- USB 2.0 Full Speed Interface
- 8 Programmable Endpoints with IN or OUT Directions for Bulk, Interrupt or Isochronous Transfers (4 end-points with double buffering of 64x2 bytes)
  - DMA Controller for fast transfers between internal DPRAM to RAM
  - 48 MHz clock for Full-speed Bus Operation

Other Peripherals

- Hardware Communication Interface Detection
- Ten I/O Ports
  - I/O 0 and I/O 1 reserved for ISO 7816, SPI and I²C communication
  - 8 General Purpose I/Os
- Programmable Internal Oscillator (Up to 35 MHz for CPU and Crypto Accelerator)
- Low Power Real Time Clock (RTC)
- Two 16-bit Timers
- Random Number Generator (RNG)
- 2-level Interrupt Controller
- Hardware DES/TDES Engine DPA/DEMA Resistant
- Hardware AES 128/192/256 Engine DPA/DEMA Resistant
- Checksum Accelerator
- CRC 16 & 32 Engine (Compliant with ISO / IEC 3309)
- 32-bit Cryptographic Accelerator (Ad-X™ for Public Key Operations)
  - RSA, DSA, ECC, Diffie-Hellman, Key Generation (thanks to Crypto Toolbox Library)

6562DS – 27Sep16

Security

- Dedicated Hardware for Protection Against SPA/DPA/SEMA/DEMA Attacks
- Advanced Protection Against Physical Attack, including Active Shield, Enhanced Protection Object, CStack Checker, Slope Detector, Parity Errors
- Environmental Protection Systems
- Voltage Monitor
- Frequency Monitor
- Temperature Monitor
- Light Protection
- Secure Memory Management/Access Protection (Supervisor Mode)

Development Tools

- Voyager Emulation Platform (ATV4+) to Support Software Development
- IAR Embedded Workbench® V5.40 Debugger or Above
- Software Libraries and Application Notes

Certifications / Standards

- CC EAL4+ (Ready)

USB 2.0

Description

The AT90SO128 is a low-power, high-performance, 8-/16-bit microcontroller with ROM program memory, EEPROM memory, based on RISC architecture microcontroller.

By executing powerful instructions in a single clock cycle, the AT90SO128 achieves throughputs close to 1 MIPS per MHz. Its Harvard architecture includes 32 general-purpose working registers directly connected to the ALU, allowing two independent registers to be accessed in one single instruction executed in one clock cycle.

In addition to the 288K Bytes of embedded ROM, the AT90SO128 includes 128K Bytes of high density EEPROM.

The ability to map the EEPROM in the code space allows parts of the program memory to be reprogrammed in-system. This technology combined with the versatile 8/16-bit CPU on a monolithic chip provides a highly flexible and cost-effective solution to many applications.

The USB V2.0 Full Speed controller provides a dynamic pull-up attachment and detachment and a host detection mechanism. It requires a 48 MHz external crystal for the data transfer.

The USB interface provides eight configurable data transfer endpoints, each with its own DPRAM in the memory area. The data transfer type for each endpoint is configured by software. A DMA controller allows a fast communication rate between the RAM of the CPU and the DPRAM.

The High Speed SPI, when configured as a master, provides a clock up to 20MHz thanks to the dedicated internal VFO clock system. A specific DMA contoller allows fast tranfers between DPRAM banks to CPU RAM. The internal DPRAM memory provides 4 DPRAM buffers of 16 bytes each. The SPI controller features three sources of interrupt (Byte Transmitted, Time-out and Reception Overflow) and a programmable clock and inter-bytes (guardtime) delays.

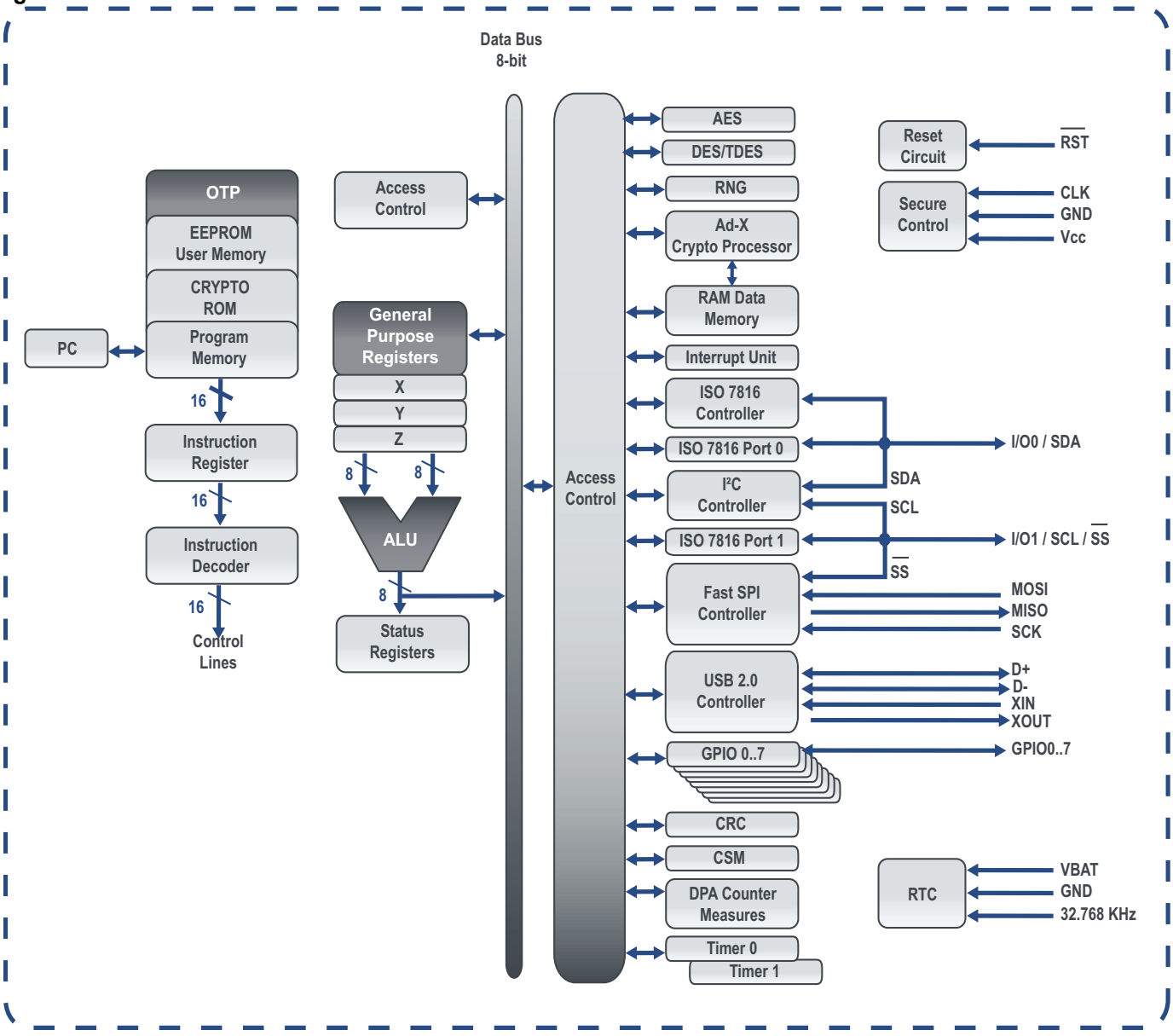
The I²C interface interconnects components on a unique two-wire bus, made up of one clock line and one data line with speeds of up to 400 Kbits per second, based on a byte-oriented transfer format. It is programmable as a master or a slave with sequential or single-byte access. Multiple master capability is supported. Arbitration of the bus is performed internally and puts the I²C in slave mode automatically if the bus arbitration is lost.

Ordering information

Reference	Description
AT90SO128-xxx-P	**xxx** : Chip Personalization Number* **P** = Z : QFN44 Package R : SOIC8 Package

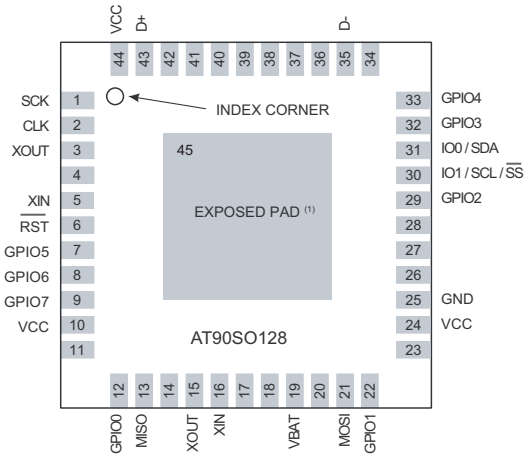
* For more details about the Chip Personalization Number, please contact your local INSIDE Secure sales office.

Figure 1 AT90SO128 RISC RISC CPU Core Architecture



Pinouts & Packages

Figure 2 AT90SO128 pinout - QFN44 package



(1)The exposed pad is internally connected to the ground. It must be connected to GND.

Figure 3 AT90SO128 pinout - SOIC8 package - USB Configuration

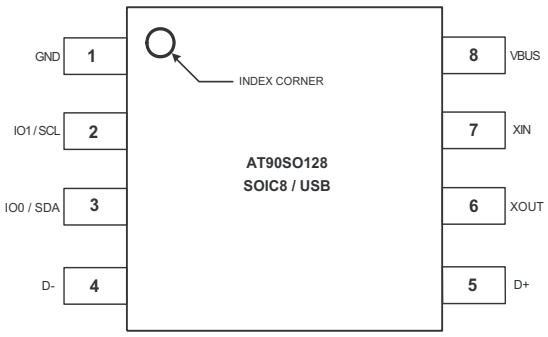


Figure 4 AT90SO128 pinout - SOIC8 package - SPI Configuration

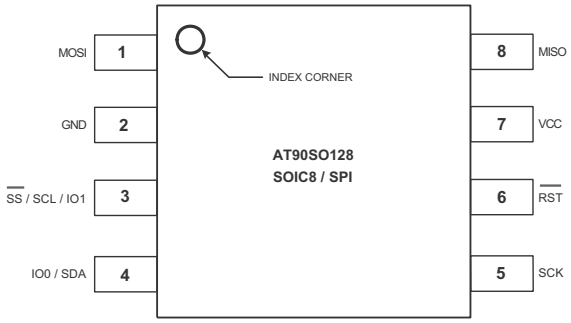


Figure 5 AT90SO128 pinout - SOIC8 package - ISO Configuration